EE/CPRE/SE 4920 - sddec24-13

ReRAM Compute ASIC Fabrication

Weekly Report 3

9/20/2024 - 10/324

Client: Prof. Henry Duwe

Advisor: Prof. Cheng Wang

Team Members:

- Gage Moorman - Team Organizer, main analog designer
- Konnor Kivimagi - Main documentation editor, mixed analog digital designer
- Nathan Cook – Main client liaison, mixed analog digital designer
- Jason Xie – Assistant documentation editor, main digital designer

Weekly summary:

After much trial and suffering precheck has finally been worked out and a tutorial has been created to help alleviate the pain for future students that work on this project. There was also progress made into creating the C code necessary for the ReRAM operations to be run by the processor.

Past Week Accomplishments:

- Solved ReRAM recheck issues and created documentation to help future users through the process.
- Have SoC code ready to test just have to setup the wrapper in the Verilog file

Individual Contributions:

Team Member	Contributions	Weekly hours	Total Hours
Konnor Kivimagi	Fixed precheck problems and created documentation for common issues	20	126
Gage Moorman	Created lookup table for MOS devices to help optimize TIA and ADC. Recalculated TIA and Comparator specs and updated schematics to meet new specifications. Trouble shooted StrongARM latch and began preping alternate soultions	12	85
Nathan Cook	Logic analyzer and GPIO pin configurations documented. Process for c test code in progress	9	80
Jason Xie	Found a method to generate combinational logic in Xschem, currently working on finishing testbench	12	83

Pending Issues:

- Gate level simulation for digital hardening is having issues
    - Having some issues correctly flattening and importing spice files into Xschem
- Having difficulty using ngspice and xschem analysis tools effectively
- Making implementation of ReRAM functions simpler so later groups can spend more time testing the array itself and not writing the software.
- Having issue with Xschemrc and ngspice identifying the correct subcircuit netlist
- StrongARM latch appears to be loading the input and not producing the correct output at Vref 12-16

Plans for the coming week:

- Gage Moorman
    - Build upon analog documentation
    - Do ADC matching analysis
    - Optimize TIA and ADC to meet 20MHz bandwidth requirements
- Konnor Kivimagi
    - Simulate ReRAM design after a succesful LVS run to verify it still functions as intended
    - Design larger ReRAM arrays and verify that they pass precheck.
    - Start working towards implementing multiple components to pass prechec together.
- Nathan Cook
    - Run logic analyzer test case
        - Create skeleton code for (annotate for modification in the future)
            - Form
            - Set
            - Reset
            - Read

        - wait
        - MAC
- Jason Xie
    - Troubleshoot Xschem issues
    - Finish Priority encoder + comparator string testbench
    - Begin TCL script for comparator string layout

Summary of Advisor Meeting:

During our meetings, we continued to hash out more of the finer details of our project including a discussion of potential issues with the ADC and whether a design change at this point in the project would be beneficial. We also cleared up some confusion on the architecture of the ReRAM on how we were labeling our input and output lines and what architecture we were going with.